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Simulation of electric properties of MFIS capacitor with BNT ferroelectric thin film using Silvaco/Atlas

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Abstract: Metal-ferroelectric-insulator-silicon (MFIS) capacitors with $Bi_{3.15}Nd_{0.85}Ti_3O_{12}$ (BNT) ferroelectric thin film were simulated using a commercial software Silvaco/Atlas, and the effects of applied voltage and insulator layer on capacitance−voltage (C−V) hysteresis loops and memory windows were investigated. For the MFIS capacitors with CeO_2 insulator, with the increase of applied voltage from 2 V to 15 V, the C−V loops become wider and memory windows increase from 0.15 V to 1.27 V. When the thickness of CeO_2 layer increases from 1 nm to 5 nm at the applied voltage of 5 V, the C−V loops become narrower and the memory windows decrease from 1.09 V to 0.36 V. For MFIS capacitors with different insulator layers (CeO_2, HfO_2, Y_2O_3, Si_3N_4 and SiO_2), the high dielectric constants can make the C−V loops wider and improve the capacitor's memory window. The simulation results prove that Silvaco/Atlas is a powerful simulator for MFIS capacitor, and they are helpful to the fabrication of MFIS nonvolatile memory devices.

Key words: MFIS; BNT ferroelectric thin film; memory window; Silvaco/Atlas

1 Introduction

Recently, ferroelectric memory field effect transistors (FEMFETs) with a metal-ferroelectric-insulator-silicon (MFIS) structure have emerged as promising nonvolatile memory devices due to their attractive properties such as nondestructive readout operation, low power consumption and high switching speed[1]. However, before they can be utilized, the electric properties of MFIS capacitors such as capacitance−voltage (C−V) characteristic and memory window need to be better understood[2]. Experimentally, there are many studies on the optimization of MFIS capacitors with different ferroelectric and insulator layers, and the electric properties are also investigated[3−4]. The 2-dimensional (2D) device simulator Silvaco/Atlas can be successfully used to simulate the electric properties of MFIS capacitors composed of n-type doped polysilicon, PZT thin film, SiO_2 insulator layer, and silicon substrate[5]. As far as we know, the electric properties simulation of MFIS capacitor with lead-free ferroelectric thin film with a bismuth-layered perovskite structure is rarely reported, although the electric properties such as the C−V characteristics and memory window are very significant for ferroelectric memory devices.

In this work, the simulation of electric properties of MFIS capacitor with $Bi_{3.15}Nd_{0.85}Ti_3O_{12}$ (BNT) thin film was performed. The effects of applied voltage and insulator layer thickness on C−V characteristics and memory windows were investigated for the CeO_2 insulator layer. The insulator layer material (CeO_2, HfO_2, Y_2O_3, Si_3N_4 and SiO_2) dependence of electric properties of MFIS capacitor was also investigated via the variations of dielectric constants and applied voltages.

2 Methodology

2.1 Detail of MFIS capacitor structure

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Schematic illustration of a MFIS capacitor structure is shown in Fig.1. The length and width are 2 μm and 1 μm, respectively, and the thickness of BNT ferroelectric layer is 200 nm. The thicknesses of metal electrode and substrate are not considered for the n-type doped polysilicon and the p-type doped silicon according to the Silvaco/Atlas instruction. To investigate the insulator layer thickness dependence of electric properties for MFIS capacitor, the insulator thickness increases from 1 nm to 5 nm. Relative parameters are listed in Table 1[4, 6−9].

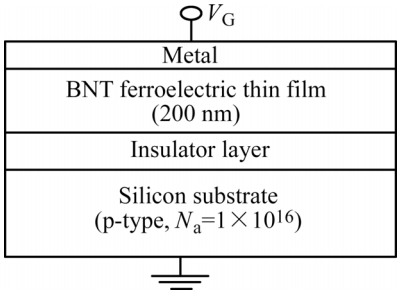

Fig.1 Schematic illustration of MFIS capacitor structure

Table 1 Device parameters used in simulation

Parameter	Definition	Value
P_r/(μC·cm^{-2})	Remnant polarization of BNT thin film	26
P_s/(μC·cm^{-2})	Spontaneous polarization of BNT thin film	32
E_c/(kV·cm^{-1})	Coercive field of BNT thin film	60
ε_f	Dielectric constant of ferroelectric layer	350
ε_{SiO_2}	Dielectric constant of SiO_2	3.9
$\varepsilon_{Si_3N_4}$	Dielectric constant of Si_3N_4	7.9
ε_{HfO_2}	Dielectric constant of HfO_2	22
ε_{CeO_2}	Dielectric constant of CeO_2	28
$\varepsilon_{Y_2O_3}$	Dielectric constant of Y_2O_3	18
t_f/nm	Thickness of ferroelectric film	200
N_a/cm^{-3}	Substrate doping concentration	10^{16}

2.2 Operation of Silvaco/Atlas software

Silvaco/Atlas consists of many models with different functions. FERRO and S-Pisces models are used. In order to consider the saturated and unsaturated polarization behavior of ferroelectric material under different conditions, the FERRO and UNSAT.FERRO models are based on the ferroelectric permittivity theoretical model proposed by Miller in Silvaco/Atlas[5, 10]. To obtain C−V hysteresis loops of MFIS capacitor under high frequency (1 MHz), the FERRODAMP parameter in FERRO model is used to illustrate the effect of the polarization of dielectric permittivity, and it is determined as 0 by analogy with the simulation[11]. Considering the work-functions of BNT thin film, semiconductor substrate and metal electrode, the contacts are set to be Schottky for the top electrode and Ohm for the bottom electrode[12]. There is Brew's charge sheet model in S-Pisces. Combined with Brew's charge sheet model and Miller's ferroelectric permittivity model, Silvaco/Atlas can be used to predict the electric properties of MFIS capacitor[11]. The model used in Silvaco/Atlas is modified from Miller's model, which can fit well with experimental data while the ferroelectric material is saturated[10]. However, if the ferroelectric material is unsaturated, the ability of this model to predict the ferroelectric behavior is poor, especially for MFIS structure[13].

3 Results and discussion

3.1 Effect of applied voltage on electric properties

The C−V characteristics and memory windows of MFIS capacitor with CeO_2 insulator layer at various applied voltage are shown in Fig.2. The thickness of CeO_2 layer is 1 nm. The inset shows the corresponding memory window as a function of applied voltage. In Fig.2, there are a flat band voltage shift and clockwise hysteresis loops, which is induced by the ferroelectric polarization[14]. The C−V loops become wider with the increase of applied voltage. The memory window is defined as the difference of the flat band voltage shift during the voltage sweeping[15]. From the inset of Fig.2, the memory window increases with the increase of applied voltage and reaches the saturated value of 1.27 V at the applied voltage of 8 V.

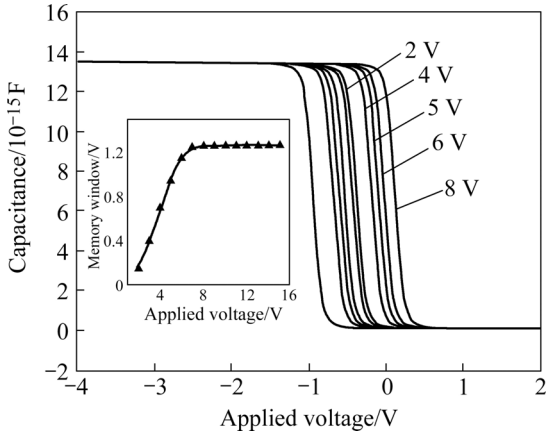

Fig.2 C−V characteristics of MFIS capacitor with CeO_2 insulator and BNT ferroelectric layers at various applied voltage(Inset shows corresponding memory window as function of applied voltage)

3.2 Effect of insulator layer thickness on electric properties

Fig.3 indicates the C−V characteristics and memory windows of MFIS capacitors with the different thicknesses of CeO_2 insulator at the applied voltage of 5 V. When the insulator thickness increases from 1 nm to 5 nm, the C−V loops become narrower and the memory windows decrease from 0.92 V to 0.31 V. They are consistent with the conventional effect of insulator thickness on electric characteristic of the MFIS capacitor[16]. The results can be understood from the relationship between the effective electric field in the ferroelectric layer and the insulator thickness. The effective electric filed in the ferroelectric layer can be expressed as[17]

$$E_f = \left(\frac{\varepsilon_i}{\varepsilon_f d_i + \varepsilon_i d_f} \right) V_G \quad (1)$$

where V_G is the applied voltage; d_f and d_i represent film thicknesses of the ferroelectric and insulator layers, and ε_f and ε_i are the dielectric constants. Obviously, E_f decreases with the increase of insulator layer thickness, and this will result in the decrease of memory window[6]. Therefore the memory window decreases with the increase of insulator thickness (see the inset of Fig.3).

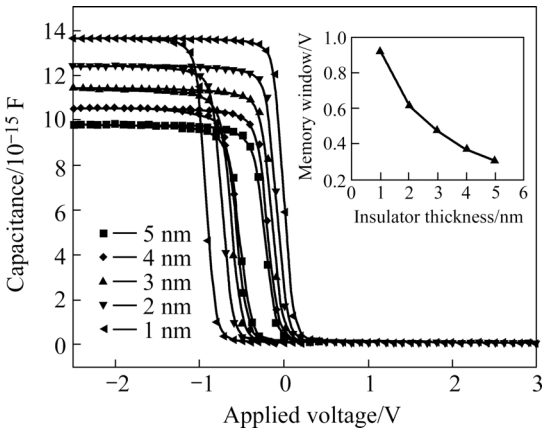

Fig.3 C−V characteristics of MFIS capacitors with different thicknesses of CeO_2 insulator layer(Inset shows corresponding memory window as function of insulator thickness)

3.3 Effect of insulator layer materials on C−V characteristics

Fig.4 shows the C−V characteristics of MFIS capacitors with different insulator layers CeO_2, HfO_2, Y_2O_3, Si_3N_4 and SiO_2, and the inset is the corresponding memory window. The insulator layer thicknesses of them are all 1 nm, and the applied voltage is 5 V. According to Fig.4 and Table 1, the C−V loops of the MFIS capacitor become wider with the increase of dielectric constant. The memory window of MFIS capacitor with CeO_2 insulator layer is 1.09 V, but the memory window is only 0.36 V for SiO_2 insulator layer. In Eqn.(1), the insulator layer with high dielectric constant ε_i will cause a higher E_f. When E_f increases, the memory window of MFIS capacitor increases[6]. Therefore the memory window increases with the increase of dielectric constant (see the inset of Fig.4).

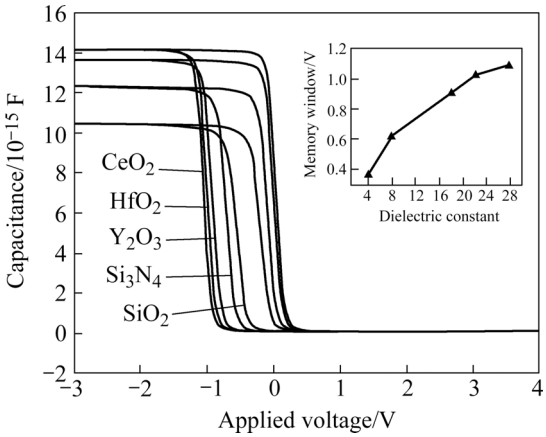

Fig.4 C−V characteristics of MFIS capacitors with different insulator layers(Inset shows corresponding memory window as function of relative dielectric constant of insulator layer)

3.4 Effect of insulator layer materials on memory windows

Fig.5 shows the memory window of MFIS capacitors with CeO_2, HfO_2, Y_2O_3, Si_3N_4 and SiO_2 insulator layers as the function of applied voltage. The memory windows of MFIS capacitors with CeO_2 and HfO_2 insulator layers are saturated at applied voltage of 7 V, whereas for MFIS capacitors with Si_3N_4 and SiO_2 insulator layers, the memory windows are still unsaturated even at applied voltage of 15 V. This means that at the same insulator thickness, the insulator layer with high dielectric constant can make the memory

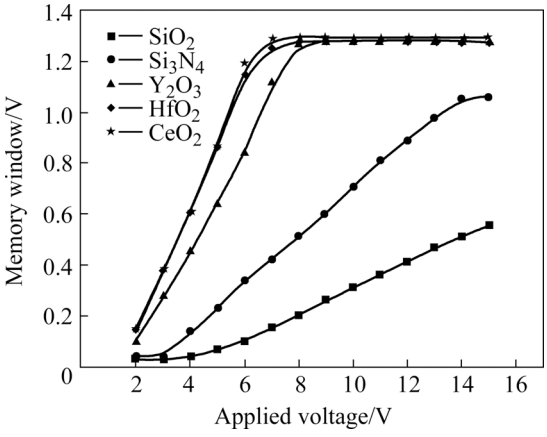

Fig.5 Memory windows of MFIS capacitors with different insulator layer as function of applied voltage

window of MFIS capacitor saturate at a lower applied voltage. This will reduce the operation voltage of the MFIS capacitor and make the device more compatible with the modern integrated circuit techniques[18].

4 Conclusions

1) The electric properties of MFIS capacitor with BNT ferroelectric thin film and various insulator layers are simulated using the 2D device simulator Silvaco/Atlas.

2) The increase of applied voltage, the decrease of insulator thickness and the enhancement of dielectric constant of insulator layer will improve the memory window of MFIS capacitor.

3) A balance should be chosen among the applied voltage, the thickness of the insulator layer and the dielectric constant of the insulator. The results will be helpful to the fabrication of MFIS nonvolatile memory devices.

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