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Microstructure and electrical properties of CeO_2 ultra-thin films for MFIS FeRAM applications

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Abstract: A detailed investigation about the dependence of microstructure and electrical properties on annealing temperature was carried out for cerium oxide(CeO_2) ultra-thin films (18 nm to 110 nm) on n-type Si(100) substrates by RF magnetron sputtering. Substrate temperature was kept constant at 400 ℃ for all samples. The as-deposited films were subsequently annealed in air ambient at 700, 800 and 900 ℃ for 1 h respectively. The crystallinity and surface morphology of the CeO_2 films were analyzed with X-ray diffractometer(XRD), scanning electron microscope(SEM), atomic force microscope(AFM) and Raman scattering measurement. Electrical properties of the Au/CeO_2/Si/Au structure were examined by high frequency capacitance—voltage (*C*—*V*) characteristics at 1 MHz and leakage current density—electric field (*J*—*E*) characteristics. A Raman peak of the CeO_2 thin films was seen at 463 cm^{-1}. From *C*—*V* data, these films exhibit dielectric constants ranging from 18 to 23, the hysteresis width (ΔV_{FB}) ranging from 0.015 V to 0.12 V and the density of trapped charges ranging from 1.45×10^{11} to 3.01×10^{11} cm^{-2}. A leakage current of 4.75×10^{-8} −9.0×10^{-7} A/cm^2 at 2 MV/cm was observed. The experimental results show that the CeO_2 buffer layers are suitable for non-volatile metal-ferroelectric-insulator-semiconductor(MFIS) structure field-effect-transistors(FETs) memory applications.

Key words: CeO_2 thin film; RF magnetron sputtering; microstructure and electrical properties; MFISFETs memory applications

1 Introduction

Recently, ferroelectric random access memory (FeRAM) has attracted much attention because of its nonvolatile operation and high access speed[1−2]. FeRAMs are classified into two types. One is one transistor and one capacitor (1T-1C) type. The other consists of metal-ferroelectric-semiconductor field effect transistor (MFSFET, e.g. 1T type)[3−6]. Compared with the 1T-1C type, MFSFET has several advantages, such as nondestructive readout and decreasing memory cell size (e.g. high-density memory devices). However, MFSFET has serious problem such as the formation of an amorphous SiO_2 layer with a low dielectric constant at the film/Si interface, highly trapped charge density and interdiffusion between the ferroelectric film and Si[7]. In order to solve these problems, a metal-ferroelectric-insulator-semiconductor(MFIS) structure was suggested by incorporating an insulator film as buffer layer between ferroelectric films and Si substrate[8]. For the applications of an insulator film to MFIS structure, several issues such as leakage current, capacitance, electrical breakdown, crystallinity, compatibility with Si, should be considered.

Among the available buffer materials, such as Al_2O_3, Y_2O_3, TiO_2, ZrO_2, HfO_2, CeO_2, and $SrTiO_3$ [9−12], cerium dioxide (CeO_2) with cubic fluorite structure (lattice parameter a_0=0.541 1 nm) has been considered one of the most important insulating material because of its desirable properties such as chemical stability and close lattice parameter matching with silicon (lattice parameter a_0=0.543 0 nm). Many physical deposition techniques, such as pulsed laser deposition(PLD)[13−14], magnetron sputtering[15], electron beam evaporation[16] and molecular beam epitaxy(MBE)[17], have been used

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to produce CeO_2 films. Several chemical methods have also been applied, such as sol-gel[18], metallorganic chemical vapour deposition(MOVCD)[19], aerosol-assisted MOCVD[20], mist microwave-plasma chemical vapour deposition(MPCVD)[21], atomic layer deposition (ALD)[22] and spray pyrolysis[23].

In this work, CeO_2 thin films (18−110 nm) were deposited by RF magnetron sputtering. Furthermore, the dependence of microstructure and electrical properties on annealing temperature of the CeO_2 thin films was investigated.

2 Experimental

A 2-inch *n*-type Si(100) single crystal wafer with 6 Ω·cm resistivity was used as a substrate. The substrate was chemically cleaned using hot solutions (80 ℃) of $\varphi(NH_4OH):\varphi(H_2O_2):\varphi(H_2O)$(=1:1:5), and φ(HCl): $\varphi(H_2O_2):\varphi(H_2O)$ (=1:1:6), and 1% HF acid. After cleaning, CeO_2 thin films were deposited on Si(100) substrates by RF magnetron sputtering method. The experimental conditions for CeO_2 thin films deposition are listed in Table 1. In order to investigate the dependence of microstructure and electrical properties on annealing temperature, the as-deposited CeO_2 thin films were annealed in air ambient for 1 h at 700, 800 and 900 ℃, respectively.

Table 1 Deposition conditions for CeO_2 thin film by RF-magnetron sputtering

Deposition parameter	Value
Substrate	n-type Si(100)
Substrate temperature/℃	400
Target (d50 mm×5.0 mm, 99.99%)	CeO_2 ceramic
Target-to-substrate distance/cm	8
Sputtering power (Forward/Reflected)/W	150/30
Gas pressure/Pa	1.3
Sputtering gas (O_2/(Ar+O_2))	1/10
Deposition rate/(nm·s^{-1})	0.6
Self-biasing voltage/V	200

XRD (Panalytical X'pert, Holland) analysis was carried out using normal 2θ scanning method, and they were scanned at 10 (°)/min with degree increment of 0.018° with Cu K_α as the incident radiation (40 kV, 10 mA). Surface morphology of CeO_2 thin films was recorded by AFM (Digital Instruments Nanoscpoe) and SEM (LEO-1530, Germany) with 50 K amplificatory. An HR 800 Raman spectrometer was conducted to study the lattice vibration modes. For electrical measurements, circular Au top electrodes (φ=0.2 mm) were sputtered on CeO_2/Si structures through a stainless steel shadow mask and Au bottom electrodes on the backside of Si using dc magnetron sputtering. The high frequency *C*—*V* characteristics were measured using an impedance analyzer (Hewlett—Packard 4192A) at a measurement frequency of 1 MHz and signal amplitude of 10 mV with the sweep rate of 0.1 V/s. Using these *C*—*V* data, interface trap densities of CeO_2/Si structures were calculated by the Terman method[24]. The leakage current density—electric field (*J*—*E*) characteristics were measured with HP4145B semiconductor parameter analyzer. All measurements were carried out at room temperature with 110 nm thick samples.

3 Results and discussion

Fig.1 shows the XRD patterns of CeO_2 thin films on Si substrates annealed at different temperatures. The films consist of (111), (220) and (311) diffraction peaks corresponding to 2θ=28.6°, 47.5° and 56.3°, respectively, indicating that the samples are polycrystalline. No other peaks belonging to other phases are detected by XRD. The intensities of all peaks increase as the temperature increases. The Raman spectra of CeO_2 thin films at different temperatures are shown in Fig.2. A well-resolved

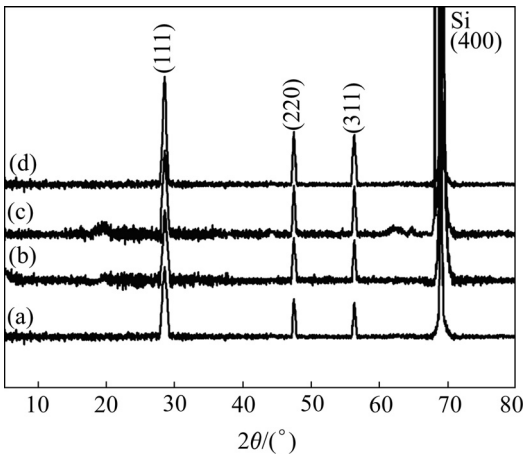

Fig.1 XRD patterns of CeO_2 thin films annealed at different temperatures: (a) As-deposited; (b) 700 ℃; (c) 800 ℃; (d) 900 ℃

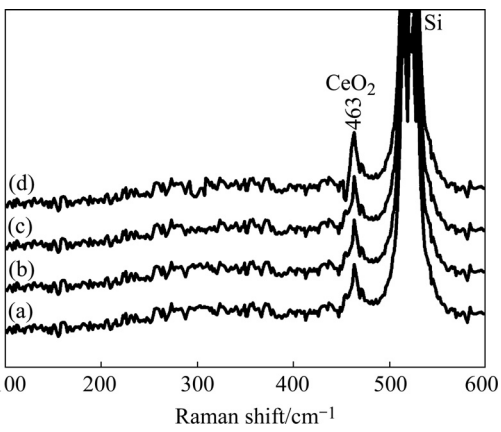

Fig.2 Raman spectra of CeO_2 thin films annealed at different temperatures: (a) As-deposited; (b) 700 ℃; (c) 800 ℃; (d) 900 ℃

Raman peak of CeO_2 thin film with grain size ranging from 20 to 41 nm is seen at 463 cm^{-1} in all samples, which is consistent with the result reported by WANG et al[25]. The intensity of peak increases slightly with increasing annealing temperature while the linewidth of peak has little change.

AFM and SEM have been employed to examine the surface morphology. Fig.3 corresponds to a typical 0.25 μm two-dimensional and three-dimensional images of CeO_2 thin film annealed at 900 ℃. Fig.3 indicates that the microstructure of CeO_2 thin film deposited directly on Si (100) substrate is granular structure with the surface roughness R_q=2.485 nm, the mean grain size is about 31.6 nm. As shown in Fig.4, the surface morphologies of CeO_2/Si thin films observed by SEM are revealed to be flat and smooth, the grain size increases with increasing annealing temperatures.

Fig.5 displays the well-behaved high-frequency *C*—*V* characteristics of CeO_2/Si structures annealed at different temperatures. A relatively little flat band voltage and small hysteresis width (ΔV_{FB}) are observed in all samples and show larger windows of the hysteresis ranging from 15 mV to 120 mV as the annealing temperature increased from 700 ℃ to 900 ℃. The dielectric constant of the CeO_2 thin films can therefore be determined from the measured value of accumulation

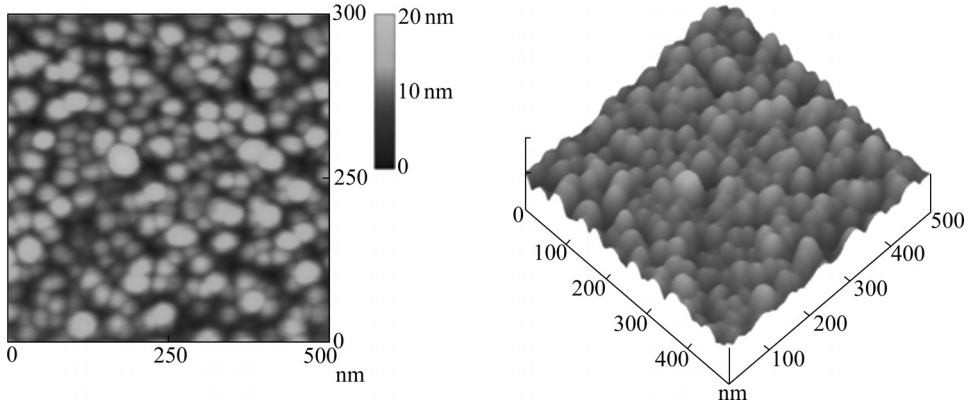

Fig.3 AFM images of CeO_2 thin film annealed at 900 ℃

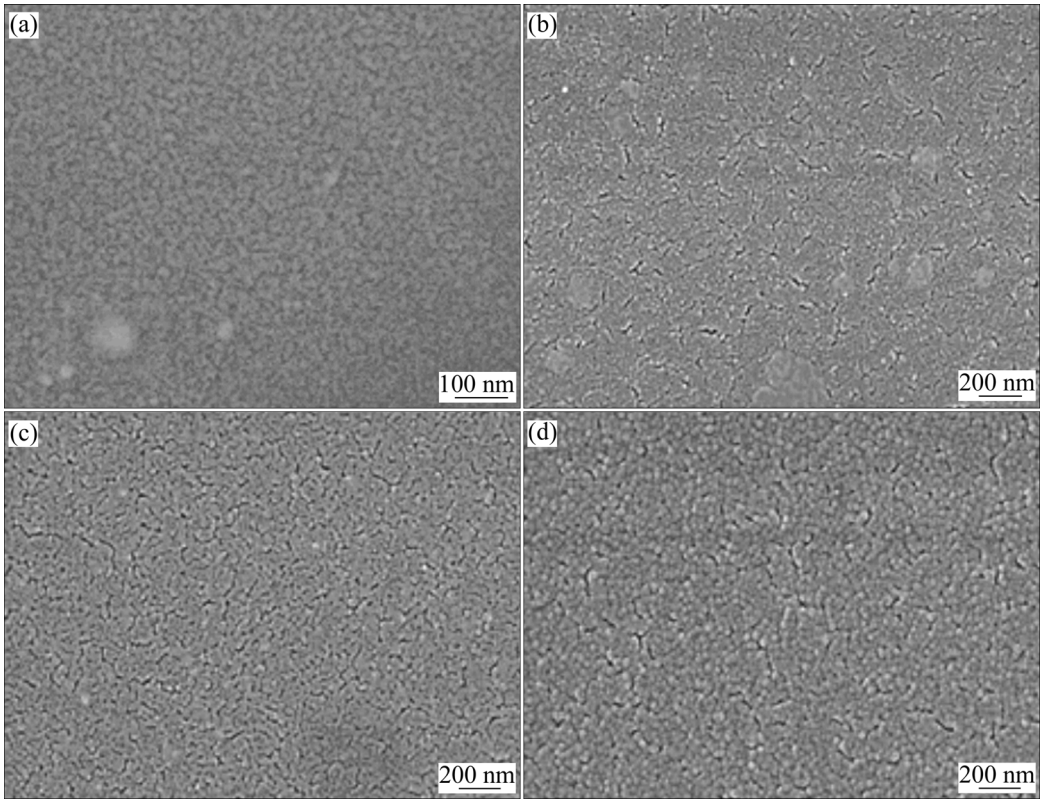

Fig.4 SEM morphologies for CeO_2 thin films on Si(100) substrate annealed at different temperatures: (a) As-deposited; (b) 700 ℃; (c) 800 ℃; (d) 900 ℃

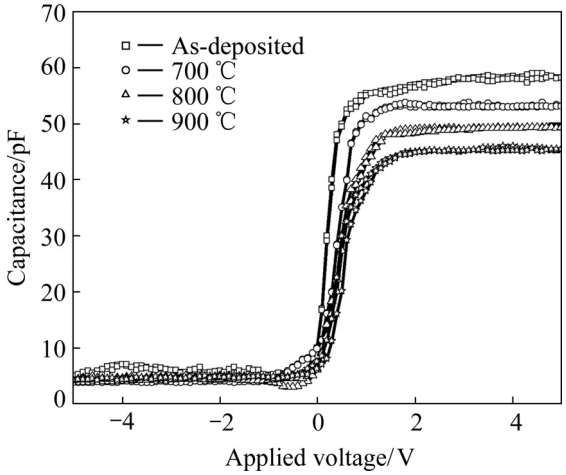

Fig.5 High frequency *C*—*V* characteristics upon different annealing temperatures

capacitance(C_{acc}), using the relation

$$C_{acc}=\frac{\varepsilon_r\varepsilon_0 A}{d} \tag{1}$$

where A is the area of capacitor(e.g. the electrode area), and d is the thickness of CeO_2 dielectric layer. The obtained ε_r value at 1 MHz ranging from 18 to 23 decreases with increasing annealing temperature, indicating the growth of the interfacial amorphous SiO_2 layer during annealing process. The equivalent oxide thickness (EOT) of CeO_2 thin films can be calculated by

$$t_{eq}=\frac{\varepsilon_{SiO_2}}{\varepsilon_r}d \tag{2}$$

where ε_{SiO_2} =3.9 is the dielectric constant of SiO_2, ε_r is the dielectric constant of CeO_2 thin films, and d is the thickness of CeO_2 thin films. The EOT increases from 18.6 nm to 23.8 nm as the annealing temperature increases. Note that for the above calculation, we ignored issues such as leakage current and reliability. In fact, actual performance of a complementary metal-oxide-semiconductor(CMOS) gate stack does not scale directly with the dielectric due to possible quantum mechanical and depletion effects[26].

Fig.6 illustrates the distribution of the four types charges: mobile ionic charge(Q_m), oxide trapped charge (Q_{ot}), fixed oxide charge(Q_f) and interface trapped charge (Q_{it}). The density of these charges should be as low as possible for the performance and reliability of MFISFET device because the presence of these charges degrades significantly several key parameters such as the threshold voltage(V_{th}), transconductance, leakage current and breakdown voltage. The density of oxide trapped charges

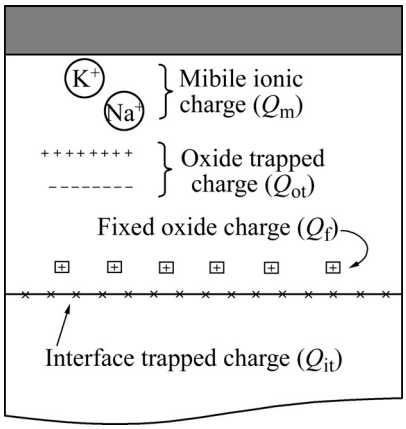

Fig.6 Distribution of four types charge in Au/CeO_2/Si(100) structure

(Q_{ot}) can be quantitatively calculated from the *C*—*V* curves using following formula as

$$Q_{ot}=\frac{C_{acc}\times\Delta V_{FB}}{qA} \tag{3}$$

where q is the electron charge. Q_{ot} increases from 1.74×10^{11} to 1.09×10^{12} cm^{-2} as the annealing temperature increases. Using the *C*—*V* data shown in Fig.5, we also calculated the interface trapped charge density (Q_{it}) by the Terman method:

$$Q_{ot}=\frac{C_{acc}\times\Delta V_{FB}}{qA} \tag{4}$$

and

$$Q_{it}=\frac{C_{ox}}{q}\frac{\mathrm{d}(\Delta V_G)}{\mathrm{d}\Phi_S} \tag{5}$$

where C_{ox} is the CeO_2 oxide capacitance per unit area, V_G is the gate bias, Φ_S is the surface potential, and C_S is the silicon surface capacitance per unit area. The calculated interface trapped charge density (Q_{it}) increases from 2.024×10^{12} eV^{-1}/cm^2 to 3.453×10^{12} eV^{-1}/cm^2 as the annealing temperature increases. We speculated that this observation may be due to the increase of the interface trapped charge density caused by increasing the internal stress in CeO_2 thin films[24].

Fig.7 shows that the leakage current density of CeO_2 thin films decreases with increasing annealing temperature. The observed leakage current density at an applied electric field of 2 MV/cm is 4.75×10^{-8} to 9.00×10^{-7} A/cm^2, breakdown fields are measured as $E_{BD}\approx3.5$ MV/cm. The decrease of the leakage current level is due to the densification of the CeO_2 thin films as well as the growth of the interfacial oxide layer.

In summary, all experimental results are listed in detail in Table 2 for integrity.

Table 2 Electrical parameters of MIS diodes with CeO_2 dielectric layer (110 nm)

Annealing temperature	ε_r	ΔV_{FB}/mV	EOT/nm	Q_{ot}/cm^{-2}	Q_{it}/(eV^{-1}·cm^{-2})	J at 2 MV·cm^{-1}/(A·cm^{-2})
As-deposited	23.0	15	18.6	1.74×10^{11}	2.024×10^{12}	9.00×10^{-7}
700 ℃	21.0	27	20.4	2.85×10^{11}	2.865×10^{12}	3.11×10^{-7}
800 ℃	19.5	55	22.0	5.40×10^{11}	3.102×10^{12}	1.02×10^{-7}
900 ℃	18.0	120	23.8	1.09×10^{12}	3.453×10^{12}	4.75×10^{-8}

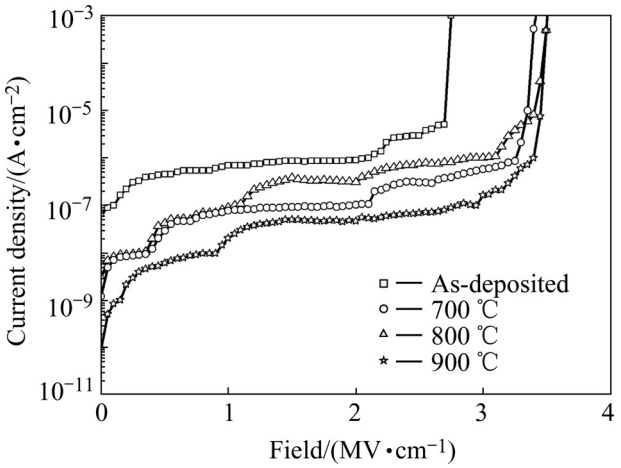

Fig.7 Leakage current density—electric field (J—E) characteristics upon different annealing temperatures

4 Conclusions

The dependence of microstructure and electrical properties on annealing temperature of CeO_2 thin films deposited by RF magnetron sputtering were investigated as an insulator of the MFIS structure. All samples (18−110 nm) were polycrystalline, and showed stoichiometric CeO_2 structure. The dielectric constant (ε_r) and leakage current density(J) decrease with the annealing temperature increasing, while the hysteresis width (ΔV_{FB}), equivalent oxide thickness(EOT), oxide trapped charges density(Q_{ot}) and interface trapped charge density(Q_{it}) increase with the annealing temperature increasing. Breakdown fields were about $E_{BD}\approx3.5$ MV/cm. The experimental results suggest that the CeO_2 buffer layers are suitable for non-volatile MFISFET memory applications.

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