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TEM study on $Si_{0.65}Ge_{0.35}$/p-Si HIP infrared detector①

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Abstract: Microstructure of P^+-$Si_{0.65}Ge_{0.35}$/p-Si HIP infrared detector has been studied by using localization cross-section transmission electron microscopy. The photosensitive region of the detector consists of 6 P^+-$Si_{0.65}Ge_{0.35}$ layers and 5 UD-Si layers, which are flat and have thickness of 6 nm and 32 nm, respectively. A stress field exists on the interface between $Si_{0.65}Ge_{0.35}$ and UD-Si layers, but no any crystal defect has been found in this region, except the edges of this region. Both $Si_{0.65}Ge_{0.35}$ and UD-Si layers on amorphous SiO_2 layer consist of polycrystals and are in wave. There is defect area in the edges of photosensitive region. The area appears in a shape of inverse triangle and the maximum width is less than 120 nm. The crystal defects are stacking faults and microtwins.

Key words: infrared detector; heterojunction semiconductor device; microstructure of semiconductor device; transmission electron microscopy
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1 INTRODUCTION

The application of infrared detectors and infrared focal plane arrays (FPA) technology are getting urgent day by day, along with the development of remote sense and telemetry science and military demands[1]. At present, the main infrared detectors used in practice are: InSb and PtSi infrared detectors working at 3 ~ 5 μm atmospheric windows, and HgCdTe infrared detector working at 8 ~ 14 μm atmospheric windows. They have their own advantages and weak points, although all of them can operate at 77 K liquid nitrogen temperature.

P^+-$Si_{0.65}Ge_{0.35}$/p-Si heterojunction internal photoemission (HIP) infrared detector offers a great deal of advantages, including easily forming monolithic integration with CMOS or CCD reading circuit, the simple technological process, lower cost, working simultaneously at both 3 ~ 5 μm and 8 ~ 14 μm atmospheric windows, high quantum efficiency compared to silicide Schottky-barrier detector, and the adjustable response wavelength. This kind of detectors has attracted great attention recently. In 1990, for the first time Lin *et al*[2] prepared a P^+-$Si_{1-x}Ge_x$/p-Si HIP infrared detector with 2 ~ 10 μm response range and 1 % quantum efficiency. In 1991, Tsaur *et al*[3] developed successfully P^+-$Si_{1-x}Ge_x$/p-Si HIP long-wavelength infrared detector arrays with 400 × 400 pixel and achieved monolithic integration with CCD reading circuit. For the infrared detector arrays, cut-off wavelength is 9.3 μm, response nonuniformity is less than 1 % and minimum resolvable temperature is less than 0.2 K.

In 1997, Wang *et al*[4,5] prepared P^+-$Si_{0.65}Ge_{0.35}$/p-Si HIP infrared detector with high quantum efficiency. The emitter of the detector was designed with stacked structure. A SiO_2 dielectric cavity and Al mirror were added in the detector and a SiO_2 anti-reflection layer was evaporated on the back of the device. Due to above measures the performance of the unbiased detector at 77 K has been improved to $D^*(5.5, 1000, 1) = 1.1 \times 10^{10}$ cm·$Hz^{1/2}$/W, the peak quantum efficiency has reached 4 % and the response range is 2 ~ 8 μm. The detector at 77 K shows ideal diode characteristics. The back leakage current density is only 10^{-4} A/cm^2. However, the performance of the device is related to its

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microstructure[6]. In this paper, the microstructures and defects of P^+-$Si_{0.65}Ge_{0.35}$/p-Si HIP infrared detectors have been studied by using cross-section transmission electron microscopy and high resolution electron microscopy.

2 EXPERIMENTAL

Normal HIP infrared detector includes a P^+-$Si_{1-x}Ge_x$ layer, as emitter, and p-Si substrate, as collector. In order to obtain higher quantum efficiency, stacking structure can be adopted[7]. The specimen in the study contains 6 P^+-$Si_{0.65}Ge_{0.35}$ layers on the p-Si substrate, grown locally by using molecular beam epitaxy (MBE) technique, and the 6 P^+-$Si_{0.65}Ge_{0.35}$ layers are separated by undoping Si (UD-Si), as shown in Fig.1. The design thickness of each $Si_{0.65}Ge_{0.35}$ and UD-Si layers are 5 nm and 30 nm, respectively. In order to efficiently restrain cross diffusion of boron and to decrease the leakage current of the detector, δ doping was used for 6 $Si_{0.65}Ge_{0.35}$ layers, that is, in every $Si_{0.65}Ge_{0.35}$ layer, the region of 1 nm thickness adjacent to Si was not doped. The doping concentration of boron in the other region is $1\times10^{20}\,cm^{-3}$.

Fig.1 Cross-section schematic of P^+-$Si_{0.65}Ge_{0.35}$/p-Si HIP infrared detector

The critical process for the detector is local growth of $Si_{0.65}Ge_{0.35}$ layer by MBE technique. A VG Semicon V80s instrument was used in the MBE processing. At first, the p-Si substrate was rinsed by using traditional cleaning method, then it was sent into pretreatment chamber and degassed at 450 ℃ for 30 min, and finally was sent into growing chamber. Before epitaxis, it was necessary to remove the thin oxide layer on the surface of p-Si substrate by heating at 950 ℃ for 15 min, which was formed at rinsing in order to prevent C and O contamination, to reveal fresh surface for epitaxis of $Si_{0.65}Ge_{0.35}$ layer. The initial vacuum in the growth chamber was 10^{-8} Pa, and the vacuum during growing was 10^{-6} Pa and the temperature of the substrate was 650 ℃. A hot boron source was used for P^+-doping and the temperature of the boron source was 1 700 ℃. The growth speed was controlled in 0.1 ~ 0.2 nm/s. The function of P^+ region shown in the left side of Fig.1 is to form good Ohm contact between aluminum electrode and Si substrate. It is considered that the defects existing in $Si_{0.65}Ge_{0.35}$ and UD-Si layers near the edge of photosensitive region will cause leakage of electricity. An N^+ zone as a protection ring was prepared to decrease the leakage of the detector near the edge.

For studying the microstructures of the detectors, we cut the detector along some direction and observed the cross-section of the specimen[8]. The preparation procedures of cross-section specimen for transmission electron microscopy (TEM) observation are the following. The wafers with devices were cut into two pieces along assigned position and adhered face to face with Gl type epoxy resin. Then the pair of wafers was cut at the appoint position by means of a low speed saw to make a slice including a detector. The slices were mechanically ground to a thickness of 20 μm by diamond powder cream and then thinned to just penetration by using ion milling instrument of Gatan 600. The ion milling current is 0.5 mA, the accelerating voltage is 5 kV, and the incident angle of ion beam is 15° ~ 12°. Because the P^+-$Si_{0.65}Ge_{0.35}$/p-Si HIP infrared detector in the study is large and has photosensitive region of 100 μm × 100 μm, the observable area of the film for TEM should be as large as possible. The interesting area (region *A*, *B* and *C*, as shown in Fig.1) should be flat and smooth and can be penetrated by electron beam in order to observe. For the observation of diffraction contrast image and high resolution image, JEM-2000FX transmission electron mi-

croscope and JEM-2010 high resolution electron microscope were used at an operating voltage of 200 kV.

3 RESULTS AND DISCUSSION

It is necessary to observe the typical regions *A*, *B* and *C* as shown in Fig.1, in order to study the microstructure of the detector and the effect on its performance. Fig.2 shows the cross-section microstructure of P^+-$Si_{0.65}Ge_{0.35}$/ p-Si HIP infrared detector. Due to the detector being larger, and the limited width of a page, so just one side image of the detector is shown in Fig.2. It can be seen from Fig.2 that the surface of p-Si substrate is flat and smooth. The corresponding electron diffraction pattern indicates that the normal direction of photograph plane is [011] and the orientation of p-Si substrate surface is [100]. Not any crystal defect has been found in the p-Si substrate. The linear pattern on the image of the p-Si substrate is extinction fringes caused by local bending of the film, which is formed during preparing specimen for TEM observation. Fig.3 shows the microstructure image of P^+-$Si_{0.65}Ge_{0.35}$/ UD-Si/ p-Si layer in photosensitive region (region *A*). In the image of photosensitive region, $Si_{0.65}Ge_{0.35}$ layers appear black and the UD-Si layers are gray. $Si_{0.65}Ge_{0.35}$ and UD-Si layers are flat and smooth. It is indicated from electron diffraction pattern and high resolution image that all these layers are epitaxial single crystal[9]. The thickness of $Si_{0.65}Ge_{0.35}$ and UD-Si layers is 6 nm and 32 nm, respectively.

Although crystal defects have not been found in P^+-$Si_{0.65}Ge_{0.35}$ layers and UD-Si layers and on their interface except the edge of this region, 2.1% mismatch exists between the $Si_{0.65}Ge_{0.35}$ and UD-Si layers. From the oscillatory contrast of $Si_{0.65}Ge_{0.35}$ layer under two beam imaging condition, as shown by black arrow in Fig.4, it can be thought that there is stress between layers. The oscillatory period of contrast is about 50 nm. Fig.5 shows multilayer structure of P^+-$Si_{0.65}Ge_{0.35}$/ UD-Si in region *C*. It is obvious that these layers consist of polycrystal. The first $Si_{0.65}Ge_{0.35}$ layer grows on the

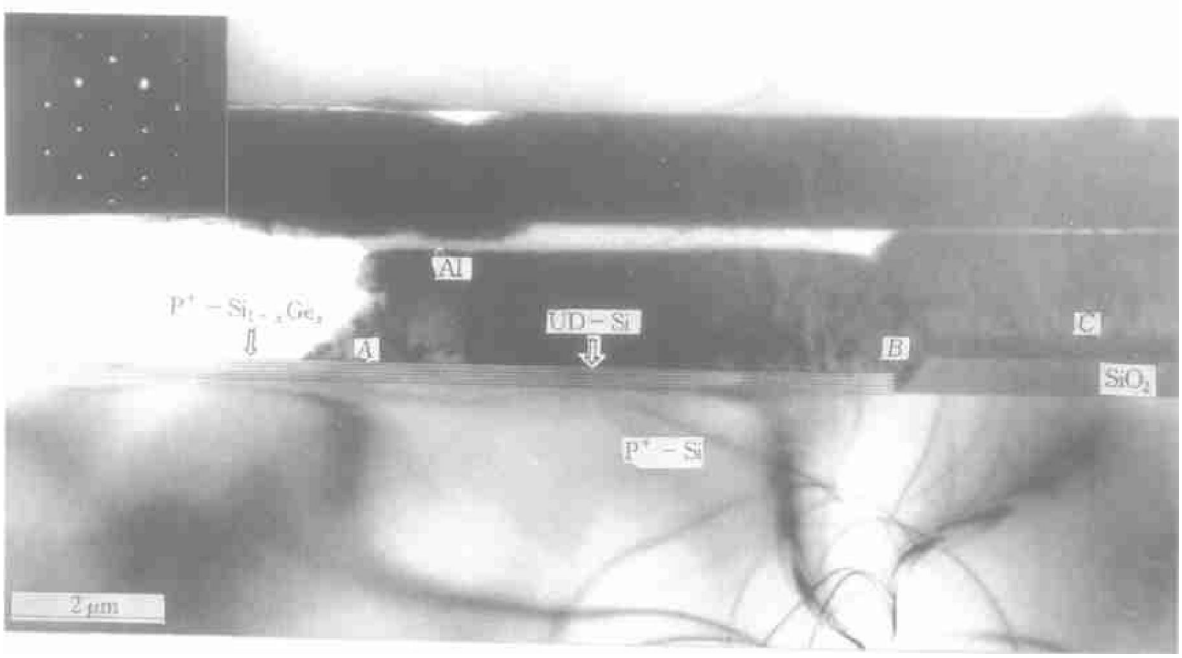

Fig.2 Cross-section microstructure image of one side of P^+-$Si_{0.65}Ge_{0.35}$/ p-Si HIP infrared detector with 6 $Si_{0.65}Ge_{0.35}$ layers

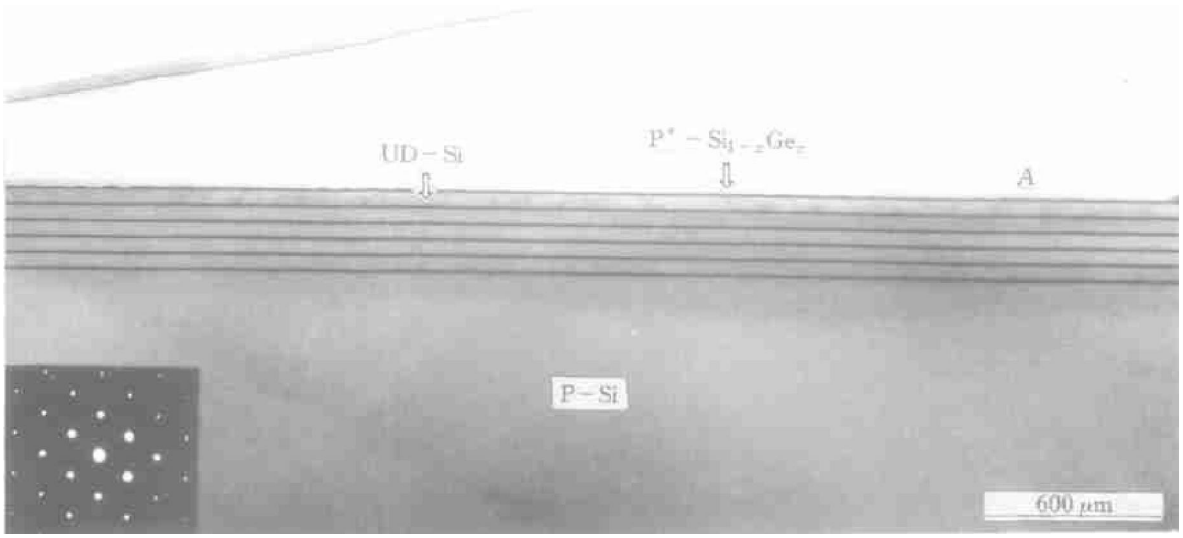

Fig.3 Image of P^+-$Si_{0.65}Ge_{0.35}$/ UD-Si layers in photosensitive region

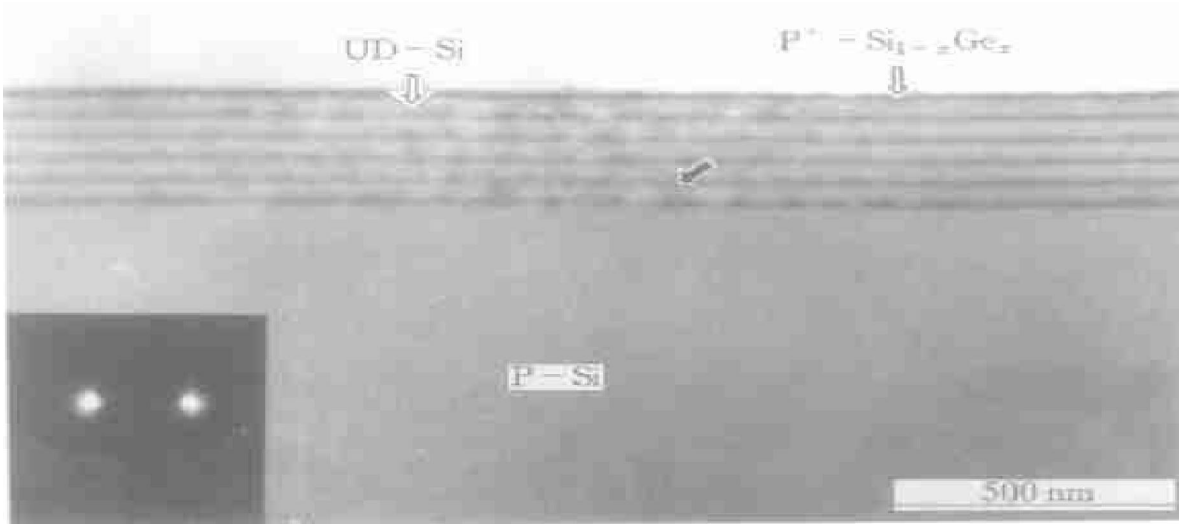

Fig.4 Diffraction contrast image of stress field between $Si_{0.65}Ge_{0.35}$ and UD-Si layers

surface of an insulating amorphous SiO_2 layer. So it is impossible to grow epitaxially, but crystals nucleate randomly on the surface of amorphous SiO_2 layer and then forms polycrystal layer. The followed UD-Si and $Si_{0.65}Ge_{0.35}$ layers grow on the first polycrystal $Si_{0.65}Ge_{0.35}$ layer. The growth speed is different with the orientation of grains in the layer, thus the followed layers form wavy polycrystal layers. This growth status can be deeply revealed by using high resolution electron microscopy.

Multilayer structure image at the slope (region *B*) of amorphous SiO_2 layer is shown in Fig. 6(a). $Si_{0.65}Ge_{0.35}$ and UD-Si layers also grow on amorphous SiO_2 layer, so these layers are polycrystal and are in wave. Due to the growth on a slope, thickness and interlayer spacing are obviously much smaller than that of level parts (regions *A* and *C*). As stated above, the single crystal layers in photosensitive region (region *A*) grow epitaxially and the layers of region *B* grow in polycrystal way. On the borders between regions *A* and *B*, the contrast image of $Si_{0.65}Ge_{0.35}$ layer thickens and curves. This

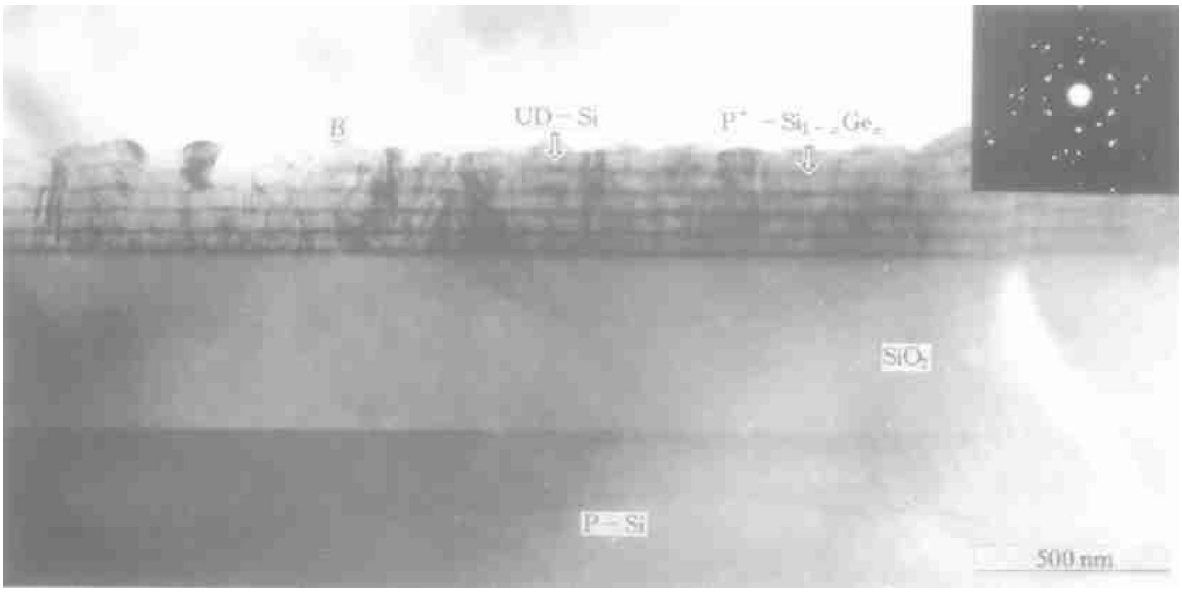

Fig .5 Image of multilayer $Si_{0.65}Ge_{0.35}$/ UD-Si on amorphous SiO_2 layer

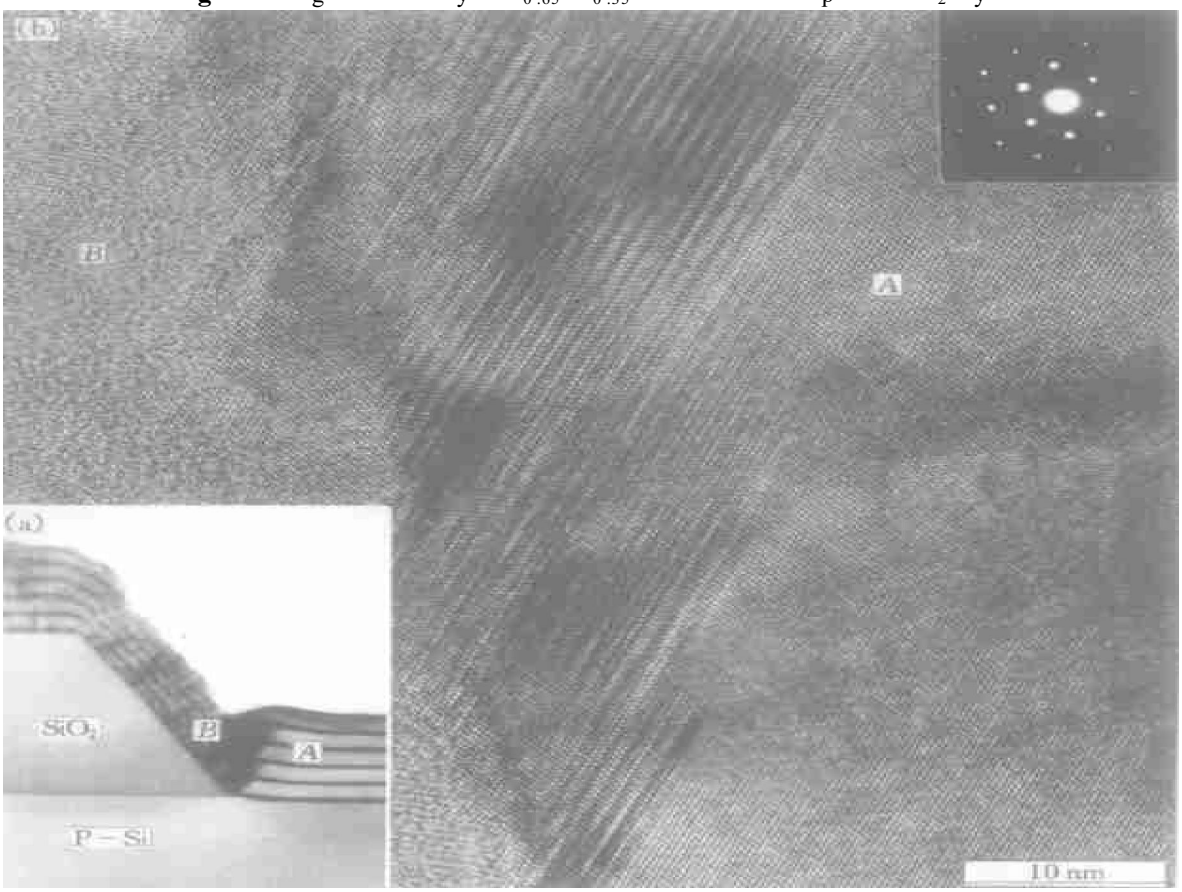

Fig .6 (a) Multilayer structure image (region *B*) on slope of amorphous SiO_2 layers; (b) HREM image at connection area between regions *A* and *B*

means that a lot of defects exist in the border between single crystal layer and polycrystal layer. The defects in the border become more and more with growing of followed layers, and the defect area is getting extensive towards inside of photosensitive region (region *A*). Fig.6(b) shows the high resolution image of the borders between regions *A* and *B*. The incidence direction of electron beam in Fig.6(b) is [011]. The defect area appears in a shape of inverse triangle and the maximum width of the area is less than 120 nm. Analysis indicates that the main defects are stacking faults and microtwins. The stacking faults are on the $(\bar{1}11)$ plane. The twinning plane is $(\bar{1}11)$ and the thickness of the most microtwins is only 2 ~ 4 times of interplanar spacing. It is obvious that the edge of photosensitive region does not have ideal perfect structure. It is very difficult to avoid defects in the borders between monocrystal region and polycrystal region during growth, but it is possible to reduce the defect area. These defects may cause electricity leakage. In order to decrease the leakage, an N^+ zone as a protection ring has been prepared inside p-Si substrate near the edge of photosensitive region, as shown in Fig.1. Although the doping in N^+ zone makes scattering factor of this zone different from other regions of p-Si substrate, the effect on scattering of incidence electron beam is so weak that the image of N^+ zone can not be observed under our imaging condition.

4 CONCLUSIONS

(1) $Si_{0.65}Ge_{0.35}$ and UD-Si layers in photosensitive region of the detector are flat and smooth, and the thickness of the layers is about 6 nm and 32 nm, respectively. At the P^+-$Si_{0.65}Ge_{0.35}$/UD-Si layer interface, stress field exists due to the effect of 2.1 % mismatch, but not any crystal defect has been found.

(2) $Si_{0.65}Ge_{0.35}$/UD-Si layers grown on amorphous SiO_2 layer appear in wave, and every layer consists of polycrystals.

(3) There are defects in the edge of photosensitive region. The maximum width of the defect area is less than 120 nm, and main defects in the area are stacking faults and microtwins. The stacking faults are on the $(\bar{1}11)$ plane. The thickness of the microtwins is only 2 ~ 4 interplanar spacing, and the twining plane is $(\bar{1}11)$.

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